WHAT IS CLAIMED IS:

Sub A1

1. A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

2. The microprocessor according to claim 1, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

3. The microprocessor according to claim1, wherein said load

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

13. The memory device according to claim 12, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

14. The memory device according to claim 12, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

15. The memory device according to claim 12, wherein the access speed of said second memory unit is faster than the access speed of said first memory unit.

16. The memory device according to claim 15, wherein said second memory unit is constituted of a synchronous DRAM.

module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

4. A microprocessor to which a plurality of memory units having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit;

a storage unit which stores an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code stored in said second memory unit.

5. The microprocessor according to claim 4, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

6. The microprocessor according to claim 4, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

7. A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memories to a logical address of a load module stored in said first memory unit;

a copying unit which copies an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and

a second address conversion unit which assigns a physical address of said second memory unit to a logical address of the instruction code copied to said second memory unit.

8. The memory device according to claim 7, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns

the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

9. The memory device according to claim 7, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

10. The memory device according to claim 7, wherein the access speed of said second memory unit is faster than the access speed of said first memory unit.

11. The memory device according to claim 10, wherein said second memory unit is constituted of a synchronous DRAM.

12. A memory device comprising:

a plurality of memory units having physical addresses different from each other;

a first address conversion unit which assigns a physical address of a first memory unit out of said plurality of memory units to a logical address of a load module stored in said first memory unit;

a storage unit which stores an instruction code from said load module stored in said first memory unit to a second memory unit out of said plurality of memory units; and